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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,410	02/09/2004	Takashi Miyazawa	118374	6611
25944 7590 01/29/2008 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850				
			EXAMINER SHANKAR, VIJAY	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 01/29/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/773,410

Applicant(s)

MIYAZAWA, TAKASHI

Examiner

VIJAY SHANKAR

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 14-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 14-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazawa (US 6,858,991 B2).

Regarding Claims 14, 18, Miyazawa teaches a method of driving an electro-optical device having scanning lines, data lines, and pixel circuits each of which includes an electro-optical element and a driving transistor, (Figures 1-10; Column 9, line 46- Col.21, line 65) the method comprising: setting a potential of a controlling terminal of the driving transistor to a first voltage level, the setting of the potential of the controlling terminal to the first voltage level including electrically connecting one of a source and a drain of the driving transistor to the controlling terminal during a first period (Figures 6-10; Column 14, line 18- Column 19, line 47); setting the potential of the controlling

terminal to a second voltage level by using a capacitive coupling occurring at a capacitive element connected to the controlling terminal, the setting of the potential of the controlling terminal to the second voltage level including applying a data voltage to the capacitor through one data line of the data lines and a switching transistor (Figures 6-10; Column 14, line 18- Column 19, line 47); and supplying a driving current or a driving voltage to the electro-optical element, the driving current or the driving voltage having a level corresponding to a conduction state of the driving transistor. (Figures 6-10; Column 14, line 18- Column 19, line 47).

Regarding Claim 15, Miyazawa teaches the method the first voltage level being a voltage level the driving transistor in an off-state. (Figs.6-10).

Regarding Claims 16, 19, Miyazawa teaches the method the pixel circuits including a plurality of group of pixel circuits each of which is disposed along one scanning line of the scanning lines, and each of the plurality of groups of pixel circuits including electro-optical elements for an identical color, and each of the plurality of groups of pixel circuits including electro-optical elements that emit an identical color. (Column 14, line 18- Column 19, line 47).

Regarding Claim 17, Miyazawa teaches the method the electro-optical element being EL element (210 in Fig.7).

Regarding Claim 20, Miyazawa teaches the method the switching transistor being included in each of the pixel circuits.(Figs.2,8).

Regarding Claims 21, 26-28,, Miyazawa teaches the electro-optical device further including power lines each of which disposed along a direction along which each of scanning lines extends; and the power lines intersecting the data lines. (Figs.7-8,10; Col.15, line 1-Col.16, line 55).

Regarding Claim 22, Miyazawa teaches the method the conduction state of the driving transistor being set according to the second voltage level.(Figs.2,8).

Regarding Claim 23, Miyazawa teaches the method the electro-optical element being electrically connected to one power line of the power lines through the driving transistor during a second period in which the supplying of the driving current or the driving voltage to the electro-optical element is carried out. (Figs.7-8,10; Col.15, line 1-Col.16, line 55).

Regarding Claims 24-25, Miyazawa teaches a method of driving electro-optical device having scanning lines, data lines, power lines and pixel circuits each of which includes an electro-optical element and a driving transistor, ,(Figures 1-10; Column 9, line 46- Col.21, line 65) the method comprising: setting a potential of a controlling terminal of the driving transistor to a first voltage level, the setting of the

potential of the controlling terminal to the first voltage level including electrically connecting one of a source and a drain of the controlling terminal during a first period (Figures 6-10; Column 14, line 18- Column 19, line 47); setting the potential of the controlling terminal to a second voltage level by a capacitive coupling, occurring at a capacitive element connected to the controlling terminal, the setting of the potential of the controlling terminal to the second voltage level including applying a data voltage to the capacitive element through one data line of the data lines and a switching transistor (Figures 6-10; Column 14, line 18- Column 19, line 47); and supplying a driving current or driving voltage to the electro-optical element, the driving current or the driving voltage having a level corresponding to a conduction state of the driving transistor during a second period (Figures 6-10; Column 14, line 18- Column 19, line 47), the electro-optical element being electrically connected to one power line of the power lines during a second period in which the supplying of the driving current or the driving voltage to the electro-optical element is carried out (Figs. 7-8, 10; Col. 15, line 1-Col. 16, line 55).

4. Applicant's arguments with respect to claims 14-28 have been considered but are moot in view of the new ground(s) of rejection.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

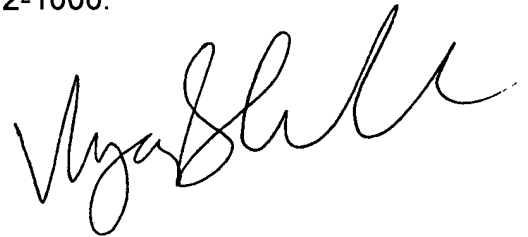
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571)272-7682. The examiner can normally be reached on M-F 7:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Vijay Shankar', is written in a cursive style.

VIJAY SHANKAR  
Primary Examiner  
Art Unit 2629

VS